IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Fernando Gonzalez et al.	§	Group Art Unit: 2815
Serial No.: 10/751,141	§	Examiner: Nguyen, Joseph H.
Filed: December 31, 2003	§	
For: Transistor Having Vertical Junction Edge and Method of Manufacturing the Same	§	Atty. Docket: MICS:0114 02-1010

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November 14, 2005 — Kerri Hyland
Date — Kerri Hyland

PRE-APPEAL BRIEF REQUEST FOR REVIEW

In accordance with the OG Notice of July 12, 2005, Applicants respectfully submit this Pre-Appeal Brief Request for Review. This Request is being filed concurrently with a Notice of Appeal.

In the Final Office Action, the Examiner rejected claim 12 under 35 U.S.C. § 102(e) as being anticipated by Michejda et al. (U.S. Patent App. No. 2002/0190344, hereinafter "Michejda"). The Examiner rejected claims 17, 18 and 22 under 35 U.S.C. § 103(a) as being unpatentable over Michejda et al. in view of Tsuchiaki (U.S. Patent No. 6,271,566, hereinafter "Tsuchiaki"). Further, the Examiner rejected claims 13-16 under 35 U.S.C. § 103(a) as being unpatentable over Michejda et al. as applied to claim 12. Still further, the Examiner rejected claims 19-21 and 23-25 under 35 U.S.C. § 103(a) as being unpatentable over Michejda et al. and Tsuchiaki as applied to claims 17 and 22. Applicants, however, respectfully submit that these rejections are improper.

Anticipation under section 102 can be found only if a single reference shows exactly what is claimed. *Titanium Metals Corp. v. Banner*, 778 F.2d 775, 227 U.S.P.Q. 773 (Fed. Cir. 1985). For a prior art reference to anticipate under section 102, every element of the claimed invention must be identically shown in a single reference. *In re Bond*, 910 F.2d 831, 15 U.S.P.Q.2d 1566 (Fed. Cir. 1990). To maintain a proper rejection under section 102, a single reference must teach each and every limitation of the rejected claim. *Atlas Powder v. E.I. du Pont*, 750 F.2d 1569 (Fed. Cir. 1984). Accordingly, the Applicants need only point to a single element not found in the cited reference to demonstrate that the cited reference fails to anticipate the claimed subject matter. Further, the burden of establishing a *prima facie* case of obviousness falls on the Examiner. *Ex parte Wolters and Kuypers*, 214 U.S.P.Q. 735 (B.P.A.I. 1979). Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent some teaching or suggestion supporting the combination. *ACS Hospital Systems, Inc. v. Montefiore Hospital*, 732 F.2d 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). Accordingly, to establish a *prima facie* case, the Examiner must not only show that the combination includes *all* of the claimed elements, but also a convincing line of reason as to why one of ordinary skill in the art would have found the claimed invention to have been obvious in light of the teachings of the references. *Ex parte Clapp*, 227 U.S.P.Q. 972 (B.P.A.I. 1985).

With the foregoing legal precedent in mind, Applicants respectfully submit that the Michejda reference does not disclose each of the elements recited in the present claims. Applicants further submit that the Tsuchiaki reference does not cure the deficiencies of the Michejda reference, as discussed below. Thus, neither of the references alone or in combination discloses each of the elements recited in independent claims 12, 17 and 22, and thus, neither of the references, alone or in combination, anticipates or renders obvious the recited subject matter.

Independent claims 12, 17 and 22 each recite, *inter alia*, a transistor comprising "a drain terminal comprising a doped polysilicon material *disposed within a first shallow cavity formed in an isolation oxide region"* and "a source terminal comprising a polysilicon material *disposed within a second shallow cavity formed in the isolation oxide region.*" Italics added.

One exemplary embodiment of the recited structure is illustrated in Figs. 3-6, which are fully described by the accompanying text in the present application. Specifically, in accordance with one exemplary embodiment, isolation oxide 58 is disposed within *trenches 52*, as illustrated in Fig. 3. Subsequently, *shallow cavities 60* are formed in the isolation oxide 58. A conductive material 64, such as polysilicon, is disposed within the cavities 60, as illustrated in Fig. 5. Finally, the structures are etched to form the source terminal 36 and the drain terminal 38 disposed within the shallow cavities 64 formed in the isolation oxide 58. As noted in the present application, the term "cavity" is often used interchangeably with the word "trench" in that they are similar structures. However, "cavity" is used in the present application to distinguish from a trench. As used in the present application, the "trench" refers to a structure formed in the substrate 50, while the "cavity" refers to structures formed in the isolation oxide 58 disposed within the trench. *See* Application, page 11, lines 16-20. As noted above, each of the present independent claims recites shallow cavities *formed in an isolation oxide region.*

The Michejda reference *does not* disclose *shallow cavities formed in an isolation oxide region.* In contrast to the subject matter recited in independent claims 12, 17 and 22 of the present application, the Michejda reference discloses a semiconductor device 100 in which doped material 170 is deposited in trenches 140, 145 *formed in the semiconductor substrate.* Isolation structures 150 are formed inside the trenches 140, 145, and doped material 170 is deposited in the substrate trenches 140, 145 on top of the isolation structures 150. *See* paras. 0033-0034; *see also* Fig. 1A.

In the Final Office Action, the Examiner stated: "Michejda et al. discloses on figure 1A a transistor comprising a drain terminal 178 comprising a doped polysilicon material (para [0034], lines 5-6 and para [0058]) disposed within a first shallow cavity formed in an isolation oxide region 150 (para [0033], lines 4); a source terminal 178 comprising a polysilicon material disposed within a second shallow cavity formed in the isolation oxide region." Final Office Action, page 2. Thus, in the Final Office Action, the Examiner analogized the isolation structures 150 in Michejda et al. to the isolation oxide region in claims 12, 17 and 22. However, in the Final Office Action, the Examiner failed to identify shallow cavities formed in the isolation structures 150 in Michejda et al. as further recited in claims 12, 17 and 22. In the subsequent Advisory Action, the Examiner directed Applicants

to the structure disclosed in Fig. 8 of Michejda. Specifically, the Examiner stated: "Michejda et al. clearly discloses in figure 8 (showing the process steps of forming the structure of figure 1A) shallow cavities 410, 415 (para [0046], line 4) formed in the isolation structure 710, 810 (para [0046], line 3 and para [0047], line 3). Note that elements 410, 415 are openings formed in the isolation structure 710, 810, and therefore considered 'shallow cavities'."

Applicants respectfully submit that the Examiner's assertions are unsupportable. That is, Michejda *does not* disclose trenches 410 and 415 "formed in the isolation structure 710, 810." The Michejda reference discloses precisely *the opposite*. That is, Michejda discloses nitride sidewall spacers 710 and isolation structures 810 *formed in the trenches 410 and 415.*

Regardless of whether the Examiner is analogizing the isolation structures 150/810 (Fig. 1A/ Fig. 8) alone with the presently recited "isolation oxide regions" or analogizing the isolation structures 150/810 (Fig. 1A/ Fig. 8) in combination with the nitride sidewall spacers 165/710 (Fig. 1A/ Fig. 8) with the presently recited "isolation oxide regions," Michejda et al. in no way discloses cavities formed *in the isolation oxide regions* as recited in claims 12, 17 and 22. As disclosed in the Michejda reference, trenches 410 and 415 are formed *in the substrate* 210. *See* Fig. 4 and paragraph [0041]. After the trenches 410 and 415 are formed in the substrate 210, *nitride wall spacers 710 and isolation structures 810 are formed in the trenches 410 and 415. See* Figs. 5-8 and paragraphs [0045] – [0047]. Finally, the polysilicon 1010 is disposed over the remaining nitride wall spacers 710 and the isolation structures 810 *within the substrate trenches. See* Fig. 10 and paragraph [0049]. It is clear from the Michejda reference that the nitride wall spacers 710, isolation structures 810 and polysilicon 1010 are each disposed within the trenches 410 and 415 formed in the substrate 210.

In sharp contrast, independent claims 12, 17 and 22 require that the doped polysilicon material be disposed *in shallow cavities in the isolation oxide region.* This distinction is an important and novel element of each of the independent claims. In order for the Examiner to establish a *prima facie* case of anticipation or obviousness, Michejda would have to disclose shallow cavities formed in the nitride wall spacers 710 and/or the isolation structures 810. However, Michejda does not disclose such a feature. There is no cavity formed in either the spacers 710 or the isolation structures 810. The Examiner analogizes the trenches 410 and 415 with the presently recited cavities. However, the trenches 410 and 415 are *not* formed

within the spacers 710 and/or isolation structures 810. Michejda teaches exactly the opposite. That is, the spacers 710 and isolation structures 810 are formed within the trenches 410 and 415. Because the trenches 410 and 415 are clearly formed *before* deposition and formation of the nitride sidewall spacers 710 and the isolation structures 810, the Examiner's position that these trenches 410 and 415 are "formed in" the sidewall spacers 710 and/or isolation structures 810 is untenable and completely contrary to the clear teachings of Michejda. There are simply no features that could conceivably be construed as trenches or cavities formed in the sidewall spacers 710 and/or the isolation structures 810. As Michejda does not disclose cavities formed in an isolation oxide region, the reference cannot possibly disclose disposing a doped polysilicon material inside the cavities formed in the isolation oxide region as further recited in claims 12, 17 and 22.

For at least the reasons set forth above, Applicants respectfully assert the Michejda reference does not disclose a transistor comprising "a drain terminal comprising a doped polysilicon material disposed within a first shallow cavity formed in an isolation oxide region" and "a source terminal comprising a polysilicon material disposed within a second shallow cavity formed in the isolation oxide region," as recited in claims 12, 17 and 22. The Tsuchiaki reference does not cure these deficiencies of the Michejda reference. Accordingly, Applicants respectfully request allowance of independent claims 12, 17 and 22, and the claims that depend therefrom.

Respectfully submitted,

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